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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,717	09/25/2003	David A. Luick	ROC920030301US1	6088

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,717	LUICK, DAVID A.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 10* is/are rejected.

7)☒ Claim(s) *3 and 7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/25/03* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings received on 9/25/03 have been accepted by the examiner.

Specification

2. The disclosure is objected to because of the following informalities:

In page 2, paragraph 0009, the phrase "upper index indictor" should be "upper index indicator".

Appropriate correction is required.

Claim Objections

3. Claim 6 is objected to because of the following informalities:

In line 8, the phrase "upper index indictor" should be "upper index indicator".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims1-2, 4-6, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kissell (US 2006/0195683 A1).

Regarding Claim 1, Kissell discloses a system in a multi-threading execution mode (multiprocessing system with a multithreading processor, Abstract) comprising:

at least one instruction register, the at least one instruction register having a thread ID indicator (ASID, stored in the TASID bits 528 of the TCStatus Register 508, paragraph 0058);

an address generator (CPU generates virtual address) having a cache index indicator (data portion) and a plurality of cache index bits (tag portion, paragraph 0141);

a cache memory (TLB 1202);

and a selector for selecting between the thread ID indicator and the cache index indicator, the selector outputting an upper index indicator, wherein when the thread ID indicator is selected by the selector (the ASID is selected based on the current processor thread, paragraph 0140), the thread ID indicator is output to the upper index indicator, and the upper index indicator is concatenated with the plurality of cache index bits to form an address for retrieving an entry from the cache memory (tag portion including virtual page address or virtual page number is concatenated with ASID... virtual memory address to make an access, the virtual memory address is concatenated with the ASID of the process making the memory access, and the result is compared with the TLB to see if a match occurs, paragraph 0141).

Regarding Claim 2, Kissell discloses the apparatus further comprising a machine state register (cpus_allowed mask), the machine state register having an enable indicator that controls the selection of the ASID. In clearing the cpus_allowed mask, the operating system is enabled to select the ASID depending on the thread (paragraph 0162).

Regarding Claim 4, Kissell discloses the apparatus wherein each thread ID indicator (ASID) further comprises a plurality of bits (ASID stored in the TASID **bits** 528 of the Tcstatus register 508, Figure 5J).

Regarding Claim 5, Kissell discloses the apparatus wherein each thread ID indicator (ASID) further comprises a single bit (ASID stored in the TASID **bits** 528 of the Tcstatus register 508 wherein bits comprise a number of single bits, Figure 5J).

Claim 6 is rejected using the same rationale as that of Claim 1.

Claim 10 is rejected using the same rationale as that of Claim 1.

Allowable Subject Matter

6. Claims 3, 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 3, The Prior Art of Record does not teach nor suggest **in the claimed combination** the address generation of claim 1 further comprising a cache-miss counter wherein the cache miss counter controls the selection of the thread ID.

Regarding Claim 7, The Prior Art of Record does not teach nor suggest **in the claimed combination** the address generation of claim 6 wherein the step of selecting an upper index indicator further comprises the steps of: checking an enable cache indicator in a machine state register; if the enable cache indicator is set, selecting the thread ID bit; and if the enable cache indicator is not set, selecting the cache index indicator.

Regarding Claim 8, The Prior Art of Record does not teach nor suggest **in the claimed combination** the address generation of claim 6, wherein the step of selecting an upper index indicator further comprises the steps of: counting cache misses; if the number of cache misses exceeds a predefined limit, selecting the thread ID bit; and if the number of cache misses is less than the predefined limit, selecting the cache index indicator.

Regarding Claim 9, The Prior Art of Record does not teach nor suggest **in the claimed combination** the address generation of claim 6, wherein each instruction register further comprises a stream ID indicator, wherein the step of selecting an upper index indicator further comprises the steps of: checking a valid indicator and the stream ID indicator of the at least one instruction register; and if at least one instruction register having both the valid indicator and the stream ID indicator set, selecting the thread ID bit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 25, 2006

Midys Rojas
Examiner
Art Unit 2185

MR

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100